Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1. (Cancelled)

Claim 2. (Currently Amended) ~~The error detector according to claim 1, further~~ An error detector comprising:

an input port to receive encoded data;

an error checking unit to identify an error detection bit within the encoded data and to determine whether the error detection bit is valid; and

a data rate determination unit ~~adapted~~ to determine the data rate of the encoded data.

Claim 3. (Currently Amended) The error detector according to claim 2, wherein said error checking unit is ~~adapted~~ to use an output of said data rate determination unit in identifying the error detection bit.

Claim 4. (Currently Amended) The error detector according to claim 3, wherein said error detector is ~~adapted~~ to identify an error detection codeword within the encoded data.

Claim 5. (Currently Amended) A error detector according to claim [[1]] 2, further comprising:

an error correction unit ~~adapted~~ to modify the received data in accordance with a codeword within the encoded data.

Claims 6 - 12. (Cancelled)

Claim 13. (Currently Amended) The receiver according to claim [[12]] 17, wherein the error detection unit is ~~adapted~~ to attempt to validate an identified error detection code bit.

Claim 14. (Currently Amended) The receiver according to claim 13, further comprising:

an error correction unit ~~for altering~~ to alter the encoded data block in accordance with the error detection code bit.

Claim 15. (Currently Amended) The receiver according to claim 14, further comprising:

a decoder ~~adapted~~ to decode the encoded data block.

Claim 16. (Original) The receiver according to claim 15, wherein the decoder has error correction capabilities.

Claim 17. (Currently Amended) ~~The receiver according to claim 12, further~~ A receiver comprising:

an error detection unit to examine an error correction encoded data block for an error detection code bit;

a demapper coupled to said error detection unit to receive the output of the error detection unit; and

a rate determination unit ~~adapted~~ to determine the encoded data blocks data rate.

Claim 18. (Currently Amended) The receiver according to claim 17, wherein the error detection unit ~~receives~~ is to receive data rate information from said data rate determination unit and ~~examines~~ is to examine the encoded data block in accordance with the data rate information.

Claim 19. (Original) The receiver according to claim 18, wherein the encoded data block is passed to said demapper when no errors are detected, to said error correction unit when errors are detected and the data block's data rate is greater than one half, and to said decoder when errors are detected and the data block's data rate is below one half.